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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/131,846
Filing Date: July 24, 1998
Appellant(s): DENNING ET AL.

Andrew J. Dillon
Reg. No. 29,634
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed August 5, 2005 appealing from the Office action mailed March 8th, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,701,409	Gates	12-1997
PCI Local Bus Specification	Chapter 4	12-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Gates (United States Patent No. 5,701,409).

As per claim 1, Gates discloses:

specifying said hardware fault to simulate (column 2, lines 49-53: describes the loading of a command to deliberately cause a fault);

determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card (column 3, lines 38-46);

creating an analog voltage signal representative of said specified hardware fault utilizing a digital-to-analog voltage converter (column 3, lines 26-38; the digital-to-analog voltage converter as described by Applicant is inherent to the PCI specification); and

outputting said analog voltage signal during operation of said expansion card, wherein said hardware fault occurring on said expansion card is simulated (column 3, lines 26, 28)

As per claim 2, Gates discloses:

wherein said step of determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises the step of determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card (column 3, lines 26-28: the error to be simulated is an incorrect parity).

As per claim 3, gates discloses:

further comprising the step of prior to outputting said analog voltage signal, determining a proper response of said system to said hardware fault (column 4, lines 12-18, 32-46, 54-64).

As per claim 4, Gates discloses:

further comprising the step of in response to outputting said analog voltage signal, determining if said system responded properly to said hardware fault (column 3, lines 15-22).

As per claim 5, Gates discloses:

further comprising the step of determining a line of said bus which is associated with said hardware fault (column 4, lines 58-64 and column 5, lines 8-62).

As per claim 6, Gates discloses:

further comprising the step of outputting said analog voltage signal during operation of said expansion card utilizing said line of said bus (column 4, lines 58-64).

As per claim 7, Gates discloses:

further comprising the step of determining a test voltage level for said analog voltage signal, wherein said test voltage level is is a voltage level required to simulate said fault (column 4, lines 58-64).

As per claim 8, Gates discloses:

further comprising the step of outing said analog voltage signal having said test voltage level during operation of said expansion card utilizing said line of said bus (column 4, lines 58-64).

As per claim 9, gates discloses:

wherein the step of determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises the step of determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card (column 4, lines 58-64).

Claims 10-18 are directed to the data processing embodiment of the method for simulating a hardware fault of claim 10-18 are and rejected on the same grounds.

(10) Response to Argument

First, Applicant provides a description of the Gates reference identical to the description provided in the Appeal of September 27th, 2001 on page 4. This brief description will be expanded upon as needed throughout the Examiner's Answer.

Second, Applicant disembodies a quotation from the Affirming Board Decision of June 30th, 2005. Applicant uses this quotation as justification for the amended claims.

The Examiner believes that the PCI interface inherent to Gates performs the claimed functionality of the "digital-to-analog voltage converter." Column 4, line 1 of Gates states "Integrated circuit 100 includes a plurality of bus interface terminals 103-107 and a bus error generation circuit..." Interface terminals are used when transferring data from one analog domain in which digital data processing occurs to a different analog domain in which transmission occurs, for instance from a high speed, low noise silicon-based field effect transistor network to slower speed, high noise copper-based PCI bus. Gates mentions, in passing, the use of a PCI interface to carry out this operation, as to one of ordinary skill in the does not need a complete and thorough explanation of how interfaces work (column 4, lines 11-31).

The Examiner points out, Applicant's own specification assigns this functionality to the DAC, the associated relays and the associated buffers at pages 7, line 26 through page 8, line 4. The PCI specification provides a very rigorous set of parameters for how the analog voltage signals representing data may be constructed (Chapter 4, of the PCI specification discusses these parameters). Applicant does not claim or disclose the structure or manner of internal operation of the "digital-to-analog voltage converter." This makes the PCI interface and "digital-to-analog voltage converter" functionally equivalent in the claims. Thus the Examiner believes PCI interface as taught by Gates carries out the claimed limitation of "creating an analog voltage signal representative of said specified hardware fault."

Applicant argues that the XOR logic's digital output of Gates is proof positive that the PCI interface logic is totally and completely inconceivable that the PCI interface is used for "creating an analog voltage signal representing said hardware fault..." Gates clearly shows the digital logic signal of the XOR gate being supplied to pin 106 or "PAR bus terminal" 106 which is a PCI bus interface element. The XOR of Gates performs the step of "determining a signal to output utilizing said bus to simulate said hardware fault". This signal is the not the "analog voltage signal" as claimed, but the digital domain signal, which when converted by the PCI interface becomes an "analog voltage signal." Applicant, by pointing out the XOR, has in fact shown precisely why the PCI bus interface, is functionally identical to the claimed digital-to-analog voltage converter. The PCI interface is clearly shown interposed to between the output of the XOR gate and the PCI bus, which means the signal must be properly conditioned by the PCI interface for transport across the PCI bus. In summary, the XOR transmits the information necessary for the PCI interface to generate an analog voltage signal indicative, just as Applicant has claimed.

Finally, the Examiner points out that Applicant has repeatedly referred to a "digital-to-analog converter" in the Appeal Brief, while a "digital-to-analog voltage converter" has been claimed. This is important to note. A "digital-to-analog converter" is used to take number and output an analog signal, for example taking digitally sampled music and playing it via a digital-to-analog converter through a speaker driver to produce a sound wave. A "digital-to-analog voltage converter" is used to condition

digital data with one set of analog properties for unsuitable transmission to the same digital data with a different set of analog properties suitable for transmission, for instance taking the digital video signal from co-axial cable line and transforming the digital signal's analog properties to allow processing by the digital cable set top box.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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